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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/512,978	02/24/2000	Robert Kerr	MI22-1343	5932

21567 7590 08/01/2003

WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER

CAO, PHAT X

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 08/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/512,978

Applicant(s)

KERR ET AL.

Examiner

Phat X. Cao

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 May 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 51-59, 62-64 and 66-74 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 59, 62 and 69-71 is/are allowed.
- 6) ☒ Claim(s) 51-58, 63, 64, 66-68 and 72-74 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. The cancellation of claim 65 in Paper No. 19 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 51-54 and 63-64 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (US. 5,895,939) in view of Krivokapic et al (US. 6,008,094).

With respect to claims 51, 63-64 and 72, Ueno (Fig. 6) discloses an integrated circuit comprising: a semiconductor substrate 63; a diffusion region 65 formed within the substrate, the diffusion region 65 and substrate 63 forming a junction; a conductive gate line 67 formed over the substrate and diffusion region, a portion of the conductive gate line 67 over the diffusion region 65 comprising an entirety of the lateral width of the conductive gate line 67 received directly over the diffusion region; and wherein the junction is configured to be reverse biased to preclude electrical shorting between the conductive line 67 and the substrate 63 for selected magnitudes of current provided through the conductive line (column 9, lines 65-67 through column 10, lines 1-2).

Ueno does not disclose more than one conductive gate lines having a uniform lateral width and comprising equal lateral spacing between adjacent conductive gate lines.

However, Krivokapic (Fig. 4) teaches the forming of a MOS device comprising a plurality of conductive gate lines L having a uniform lateral width L_g and equal lateral

spacing between adjacent conductive gate lines. Accordingly, it would have been obvious to modify Ueno's device by forming more than one conductive gate lines having the structure as set forth above in order to form a logic gate having symmetrical gate regions, as taught by Krivokapic (column 4, lines 43-51).

With respect to claims 52-54, Ueno's Fig. 6 further discloses the diffusion region 65 comprises two portions disposed outwardly from directly beneath the conductive gate line, a first portion outward of a first side of the conductive line and a second portion outward of a second side of the conductive line.

4. Claims 55-58 and 66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komatsu et al (US. 4,516,147) in view of Wolf (vol. 3).

With respect to claims 55-57, Komatsu (Fig. 4) discloses an integrated circuit comprising: a semiconductor substrate having P-type base region 44; an emitter diffusion region 45 of N-type formed within the base region of the substrate, the emitter diffusion region 45 and the base region 44 of the substrate forming a junction; a conductive line 48E formed over the substrate and the diffusion region; a conductive material 49E interconnecting the conductive line 48E and the diffusion region 45; an entirety of the conductive material 49E received directly over the diffusion region and a portion of the entirety of the conductive material 49E being in contact and laterally spaced from the conductive line 48E; wherein the diffusion region 45 comprises at least two portions disposed outwardly from directly beneath the combined cross-sectional area of the conductive material 49E and the conductive line 48E.

Komatsu does not specifically disclose that the emitter diffusion region and the base region of the substrate forming a reverse biased junction for selected magnitudes of current provided through the conductive line.

However, Wolf teaches the obviousness of using n and p dopants in four different MOSFETs configurations, formation of pn junction and reverse biasing a pn junction of the diffusion region and the substrate by selectively apply magnitudes of voltage provided through the conductive gate line of MOSFET (see Fig. 4-2 on page 137 and related text, on page 136, section 4.1.1). Accordingly, it would have been obvious to form a reverse biased pn junction between the emitter diffusion region and the base region of the substrate for selected magnitudes of voltage on current provided through the conductive base line and the conductive emitter line of Komatsu's transistor because according to Wolf, this is a basis operation of a transistor (i.e., MOS, BJT) when the transistor is in OFF mode.

With respect to claims 66-67, recitation to the conductive line comprising "two conductive layers" fails to distinguish over Komatsu's conductive line 48E, which can be arbitrarily subdivided into numerous sub-layers about each other.

With respect to claim 58, forming metal for the conductive material of Komatsu would have been obvious because metal is a known material for providing the electrical contacts.

With respect to claim 68, Komatsu's Fig. 4 further discloses that the conductive material 49E extends on both sides of the conductive line 48E to form sidewall spacers adjacent respective sides of the conductive line 48E.

5. Claims 73-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno and Krivokapic et al as applied to claim 51 above, and further in view of Yen (US. 5,965,924).

The combination of Ueno and Krivokapic does not disclose an insulative layer having contact openings formed over the conductive lines.

However, Yen (Fig. 3B) teaches the forming of an insulating layer 76 over a diffusion region 70 and over the conductive gate line electrode 74, and the forming of a contact opening 80 through the insulative layer and over the conductive gate line electrode. Accordingly, it would have been obvious to form an insulative layer over the plurality of diffusion regions and over the plurality of conductive lines, and to form the contact openings through the insulative layer to the conductive gate lines because such contact openings are well known to one skilled in the art for providing the electrical contacts to the conductive gate lines, as taught by Yen (column 4, lines 4-10).

Allowable Subject Matter

6. Claims 59, 62, and 69-71 are allowed.

The prior art of record fails to disclose the combination of the device structure recited, including a second portion of the conductive material contacting the diffusion region at only one location.

Response to Arguments

7. Applicant argues that Krivokapic teaches away from forming a logic gate having symmetrical gate regions.

Applicant's argument is not persuasive because of the following reasons:

- first, Applicant should be aware that disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments, nonpreferred embodiments constitute prior art. *In re Susi*, 169 USPQ 423 (CCPA 1971). In this case, although Krivokapic may not prefer the forming of a logic gate having symmetrical gate

regions as suggested by Fig. 4, the artisan aware of the teachings of Krivokapic's Fig. 4 would have recognized the obviousness of forming more than one conductive lines to Ueno's device structure in order to form a logic gate having symmetrical gate regions;

- second, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation of forming a logic gate comprising a plurality transistors having symmetrical gate regions would motivate one skilled in the art to combine the references as suggested.

Applicant further argues that the combination of the prior art will change the principle operation of Ueno's transistor.

This is incorrect because Krivokapic is relied on only for teaching the known feature of forming a device having more than one transistors in its structure for the intended use purpose. Therefore, the operation of Ueno's transistor would not be changed because there is nothing change in Ueno's transistor structure. Furthermore, Applicant is reminded that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; not is it that the claimed invention must be expressly suggested in any one or

all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). The Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teachings, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

With respect to Komatsu, Applicant argues that Komatsu does not suggest a portion of the entirety of the conductive material 49E laterally spaced from a conductive line 48E.

This argument is not persuasive because Komatsu's Fig. 4 clearly discloses that the conductive material 49E has a side portion being in contact with the diffusion region 45 and the sidewalls of the conductive lines 48E, and being laterally spaced from the sidewalls of the conductive line 48E.

Regarding claims 66-67, Applicant fails to point out why the conductive line of Komatsu in the final structure distinguishes from the conductive line comprising two conductive layers as claimed.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

Art Unit: 2814

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Application/Control Number: 09/512,978

Page 9

Art Unit: 2814

PC

July 25, 2003

A handwritten signature in black ink, appearing to read 'Phat X. Cao', written in a cursive style.

PHAT X. CAO
PRIMARY EXAMINER